

CIRCUIT AND METHOD FOR INSTRUCTION COMPRESSION  
AND DISPERSAL IN WIDE-ISSUE PROCESSORS

ABSTRACT OF THE DISCLOSURE

There is disclosed bundle alignment and dispersal circuitry  
for use in a data processor. The data processor comprises: 1) C  
execution clusters, each of the C execution clusters comprising an  
instruction execution pipeline having N processing stages for  
executing instruction bundles comprising from one to S syllables,  
wherein each the instruction execution pipelines is L lanes wide,  
each of the L lanes for receiving one of the one to S syllables of  
the instruction bundles; 2) an instruction cache for storing a  
plurality of cache lines, each of the cache lines comprising C\*L  
syllables; 3) an instruction issue unit for receiving fetched ones  
of the plurality of cache lines and issuing complete instruction  
bundles toward the C execution clusters; and 4) alignment and  
dispersal circuitry for receiving the complete instruction bundles  
from the instruction issue unit and routing each the received  
complete instruction bundles to a correct one of the C execution  
clusters as a function of at least one address bit associated with  
each of the complete instruction bundles.